400G-SR4 QSFP-DD Transceiver

Product Features

- 4 x 100Gbps MMF optical interface
- Each electrical channel data rate up to 26.56GBaud with CDR
- Hot Pluggable
- Up to 100m link on OM4 Multi-mode Fiber
- 850nm VCSEL and PD Array Technology
- CML Compatible electrical I/O
- QSFP-DD MSA HW V6.3 Compliance
- CMIS V5.2 Compliance
- Optical connectivity via industry standard MPO/MTP terminate fiber ribbon
- MPO12 APC Optical Receptacle Type
- Monitors for VCSEL bias, transmitted power, received power, mod-ule temperature, and module power supply
- Case Operating Temperature:
- Commercial: 0 to 70ºC
- RoHS II Compliance

Product Applications

- High performance computing interconnect
- Data center

Absolute Maximum Ratings

Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Ambient Temperature	Tstg	-40	+85	ºC	Exceeding the Absolute Maximum Ratings may cause irreversible damage to the device. The device is not in- tended to be operated under the condition of simultaneous Absolute Maximum Ratings, a condition which may cause irreversible damage to the device.RH is Non-condensing condition.
Relative Humidity - Storage	RHS	0	95	%	
Relative Humidity - Operating	RHO	0	85	%	
Module Supply Voltage	VCC	-0.5	3.6	V	

Recommended Operating Conditions

Recommended Operating Conditions						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Case Operating Temperature	Tcase	0	+25	+70	ºC	Temperature Range = C
Module Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Consumption	P	-	-	8	W	Power Class 4
Module Supply Current	IIN	-	2424	-	mA	
Electrical Signal Rate	Se	-	26.5625	-	GBd	±100ppm; Each lane
Optical Signal Rate	So	-	53.125	-	GBd	±100ppm; Each lane

Electrical Characteristics

Transmitter Electrical Interfaces						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling rate	SR	-	26.5625	-	GBd	±100ppm; Each lane
Tx_Data Differential Input Voltage	VIN	-	-	900	mV	
Tx_Data Differential Input Impedance	ZIN	-	100	-	Ω	

Receiver Electrical Interfaces						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling rate	SR	-	26.5625	-	GBd	±100ppm; Each lane
Rx_Data Differential Output Voltage	VOUT	-	-	900	mV	
Rx_Data Differential Output Impedance	ZOUT	-	100	-	Ω	

Optical Characteristics

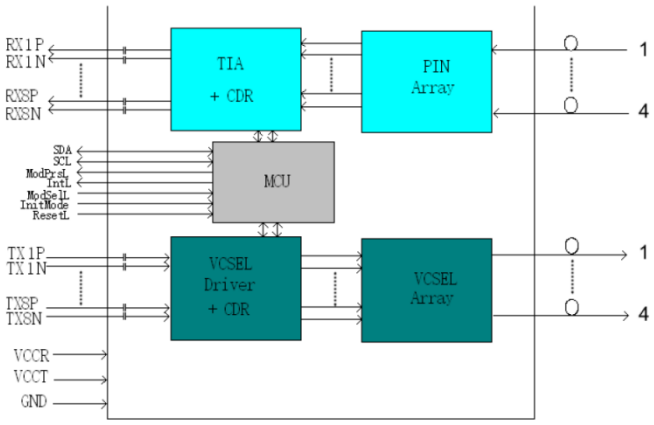
Transmitter Optical Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling rate	SR	-	53.125	-	GBd	±100ppm; Each lane
Modulation format	MF	PAM4				
Center wavelength	λ	840	-	870	nm	
RMS Spectral Width	Δλ	-	-	0.65	nm	
Average Launch Power	POUT	-4.6	-	4	dBm	Each lane

Outer Optical Modulation Amplitude	OMAouter	-2.6; –4.4 + max (TECQ, TDECQ)	-	3.5	dBm	For max (TECQ, TDECQ) ≤ 1.8 dB; For 1.8 ≤ max (TECQ, TDECQ ≤ 4.4 dB; Each lane
Transmitter and dispersion eye closure for PAM4 (TDECQ)	TDECQ	-	-	4.4	dB	Each lane
Transmitter eye closure for PAM4 (TECQ)	TECQ	-	-	4.4	dB	Each lane
Overshoot/undershoot	O/Ushoot	-	-	29	%	
Transmitter power excursion	TPE	-	-	2.3	dB	Each lane
Extinction ratio	ER	2.5	-	-	dB	Each lane
Transmitter transition time	Time	-	-	17	ps	Each lane
Average launch power of OFF transmit- ter	POFF	-	-	-30	dBm	Each lane
RIN14OMA	RIN14OMA	-	-	-132	dB/Hz	
Optical return loss tolerance	ORLT	-	-	14	dB	
Encircled flux	EF	≥86% at 19 μm; ≤30% at 4.5 μm			-	

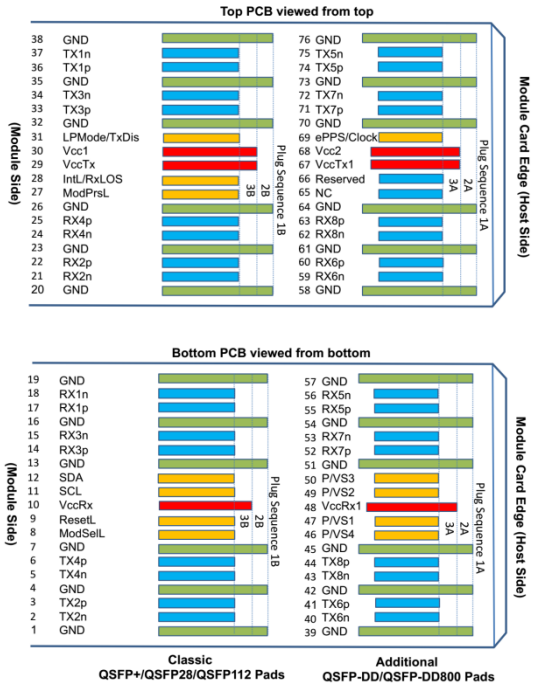
Receiver Optical Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Signaling rate	SR	-	53.125	-	GBd	±100ppm; Each lane
Modulation format	MF	PAM4				
Center wavelength	λ	840	-	870	nm	
Damage Threshold	P damage	5			dBm	
Average receive power	PIN	-6.4	-	4	dBm	Each lane; Note1
Receive power (OMAouter)	PIN (OMAouter)	-	-	3.5	dBm	Each lane
Receiver reflectance	RF	-	-	-15	dB	
Receiver sensitivity, OMAouter	Sens(OMAouter)	-	-	-4.6; -6.4 + TECQ	dBm	For TECQ≤1.8 dB; For 1.8 ≤TECQ ≤4.4 dB; BER @ 2.4E-4
Stressed receiver sensitivity (OMAouter)	Stressed-Sens (OMAoute	-	-	-2.0	dBm	BER @ 2.4E-4

	r)					
Note1: Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.						

Block Diagram



Pin arrangement

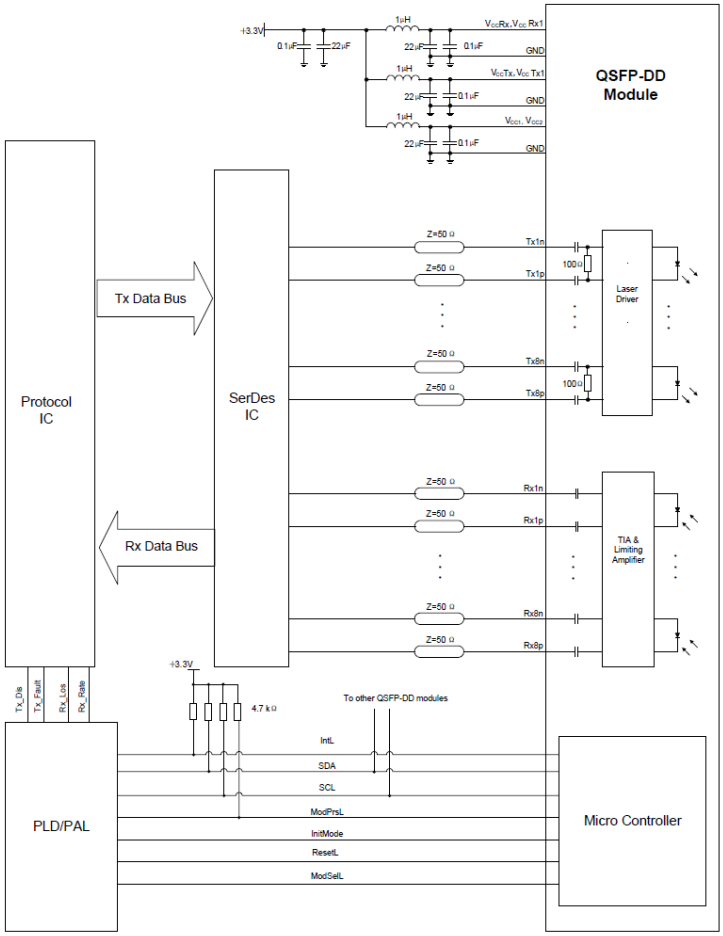


Pin Function Definitions

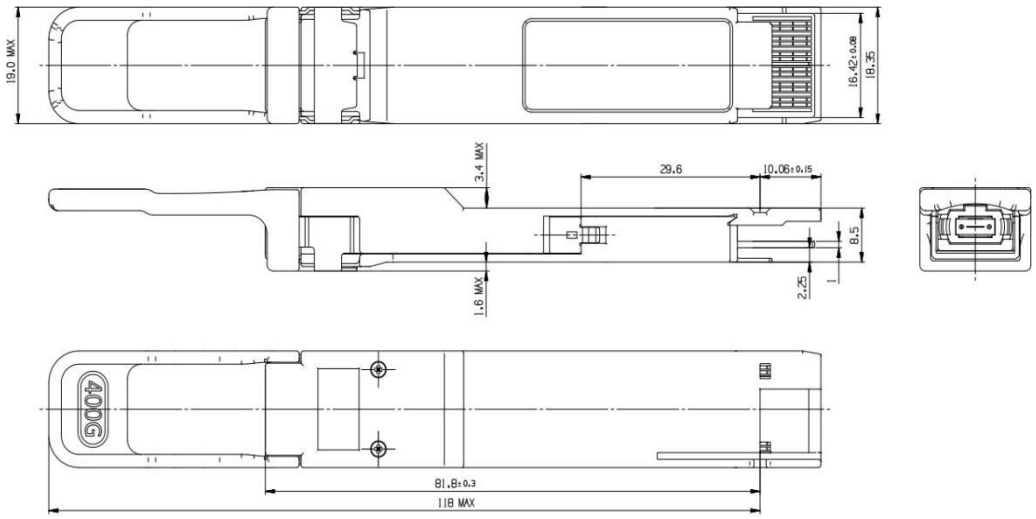
Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground

24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Electrical Interface



Mechanical Dimensions



NOTES:

1. TOLERANCE: ±0.1MM.
2. OTHERS ACCORDING WITH QSFP-DD MSA OR CUSTOMER SPEC.
3. LIGHT PORT ACCORDING WITH FIBER CONNECTOR SPEC.